A METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE HAVING A METALLIC SILICIDE LAYER

CROSS-REFERENCE TO RELATED APPLICATION

The present application claiming priority under 35 U.S.C. § 119 to Japanese Application No. 2001-354411 filed on November 20, 2001 which is hereby incorporated by reference in its entirely for all purposes.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a method for fabricating a semiconductor device which has a metallic silicide layer.

DESCRIPTION OF THE RELATED ART

In a method for fabricating a semiconductor process, a metallic silicide layer is used for a gate electrode, an active region or conductive line in order to realize lower resistance.

A self-aligned silicide (SALICIDE) method is well known as a method for

forming the metallic silicide layer. In the SALICIDE method, first a metallic layer, such as refractory metal is formed on a silicon substrate, and then plural heat treatments are carried out. Generally, a first heat treatment is for forming a metallic silicide in a surface of the substrate by diffusing a material of the metallic layer into the substrate. Other heat treatments are for reducing a resistance of the metallic silicide layer. Thereby, the metallic silicide layer can be formed in predetermined portions in the substrate by a self-aligned method.

Such SALICIDE method is disclosed in Japanese Laid-Open Patent Publication:HEI10-335261, published on December 18, 1998, Japanese Laid-Open Patent Publication:2000-82811, published on March 21, 2000, "Sub-Quarter Micron Titanium Salicide Technology With In-Situ Silicidation Using High-Temperature Sputtering" NEC Corporation, 1995 Symposium on VLSI Technology Digest of Technology Papers, p.57-58 and "The Orientation of Blanket W-CVD on the underlayer Ti/TiN studied by XRD" Toshiba Corporation Semiconductor Company, ADMETA2000:Asian Session, PS-'210, p71-72.

On the other hand, a SOI (Silicon-On-Insulator) structure having a thin

single silicon layer formed on an insulating film on a silicon substrate is well known as a structure for realizing lower power consumption.

A technique for applying the SALICIDE method to the SOI structure has been developing in order to realize both a lower resistance and lower power consumption.

A single silicon layer of a fully depleted SOI structure is very thin. Generally, a thickness of such single silicon layer is less than 50nm. In the case where a thickness of a metallic layer formed on the single silicon layer is 25nm, a thickness of metallic silicide layers formed in an active region (source and drain regions) becomes 50nm. That is, the metallic silicide layer in the fully depleted SOI structure might be contacted with the insulating film under the thin single silicon layer without making precisely adjustments to a thickness of the metallic layer formed on the single silicon layer. Such contacted area makes a contact resistance between the metallic silicide layer and the single silicon layer larger since an interface region between the metallic silicide layer and the single silicon layer becomes smaller. Further, in the case where a thickness of the metallic

layer is very thicker than that of the single silicon layer, quantity of silicon in the single silicon region is insufficient for reacting with metal in the metallic layer. As a result, voids occur in the active region due to lack of silicon in the single silicon layer.

Therefore, in the case where the SALICIDE method is applied for the SOI structure, a process for forming a thin metallic layer on the active region for forming a thin metallic silicide layer is required.

However, thin wire effect is well known in the conventional silicide process. That is, the narrower a width of the metallic silicide layer becomes, the larger a sheet resistance of the metallic silicide layer becomes. Further, the thin wire effect is remarkable in the thin metallic silicide layer.

SUMMARY OF THE INVENTION

In a preferred embodiment of the invention, a protective layer is formed on a metallic layer prior to a step for forming a metallic silicide layer, and the protective layer has a thickness thicker than that of the metallic layer.

According to the present invention, a semiconductor device having a thin

metallic silicide layer can be formed with reducing a sheet resistance by thin wire effect.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects and features of the invention and further objects, features and advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

Fig.1-Fig.5 are partial cross-sectional views describing a conventional method of fabricating a semiconductor device.

Fig.6-Fig.10 are partial cross-sectional views describing a method of fabricating a semiconductor device according to a preferred embodiment.

Fig.11(a)-Fig.11(c) are partial cross-sectional views describing various sputtering methods.

Fig.12 is a x-ray diffraction describing a relation between orientation of

(200) surface and each temperature.

Fig.13 is a relation between sheet resistance and width of silicide layers according to the preferred embodiment.

Fig.14 is a partial cross-sectional view describing a method of another preferred embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described hereinafter with reference to the accompanying drawings. The drawings used for this description typically illustrate major characteristic parts in order that the present invention will be easily understood. In this description, one embodiment is shown in which the present invention is applied to a MOS transistor.

First, an outline of a conventional process is shown in Figs.1-5. A method for forming a titanium silicide layer is described hereinafter.

A gate electrode 11 which is comprised of polycrystalline silicon having a thickness of 200nm, a gate oxide film 9 (a thickness of 10nm) under the gate electrode 11 , side walls 13 which are formed on the sides of the gate electrode 11

and field insulating layers 7 (a thickness of 400nm) are formed on a semiconductor substrate 101, as shown in Fig.1. These elements are defined as a base 111.

Then, an active region (source and drain regions; not shown) are formed by an ion implantation which introduces p type ions or n type ions into the base 111.

Then, arsenic ions As + are implanted into the base 111 at $3x10^{14}cm^{-2}$. Thereby, surfaces of the semiconductor substrate 101 become amorphous.

Next, a titanium layer 121 (a thickness of 20nm) as a metallic layer is formed on the base 111 by a sputtering method, as shown in Fig.2.

Then, a first heat treatment is carried out. That is, the base 111 on which the titanium layer 121 is formed, is heated to a temperature of 750℃ in an atmosphere of nitrogen, as shown in Fig.3. Thereby, titanium silicide layers 131, 132, 133 (a thickness of 60nm) are formed in interface surfaces. The titanium silicide layers 131, 132, 133 are respectively formed on the interface surfaces between the titanium layer 121 and the active regions and the gate electrode 11.

Such titanium silicide layers 131, 132, 133 are composed of a Ti-Si layer which has a composition ratio of titanium and silicon that is 1:1 or a Ti_2Si layer which includes more titanium than silicon. So, resistance of the titanium silicide layers 131, 132, 133 is high. That is, the titanium layers 131, 132, 133 have a crystalline structure of C49.

Then, the titanium layer 132 which is not reacted with silicon in the semiconductor substrate 101 is removed using mixture liquid of an ammonia solution and a hydrogen peroxide solution, as shown in Fig. 4.

Then, a second heat treatment is carried out. That is, the titanium silicide layers 131, 132, 133 are heated to a temperature of 850℃. Thereby, the TiSi layer or the Ti_2Si layer of the titanium silicide layers 131, 132, 133 are respectively changed into $TiSi_2$ layers 141, 142, 143, as shown in Fig.5. That is, the titaniumu layers ($TiSi_2$) 141, 142, 143 have a crystalline structure of C54. Therefore, as resistance of the titanium silicide layers 141, 142, 143 become low, resistance of the gate electrode 11 and the active regions can be reduced.

Then, an intermediate layer, contact holes and conductive lines are

formed on the base for forming MOS transistors.

Here, an outline of a process of the present invention is shown in Figs.6-14.

In this embodiment, a fully depleted SOI (Silicon-On-Insulator) structure is used.

A silicon-on-insulator (SOI) substrate which is comprised of a silicon substrate 1, a silicon oxide layer 3 on the silicon substrate 1 and a single silicon layer 5 on the silicon dioxide layer 3, is used for this preferred embodiment. A gate electrode 11 which is comprised of polycrystalline silicon having a thickness of 200nm, a gate oxide film 9 (a thickness of 10nm) under the gate electrode 11 , side walls 13 which are formed on the sides of the gate electrode 11 and field insulating layers 7 (a thickness of 100nm) are formed on the SOI substrate, as shown in Fig.6. Then, an active region (source and drain regions; not shown) are formed by an ion implantation which introduces p type ions or n type ions into the single silicon layer 5. Then, arsenic ions As^+ are implanted into the single silicon layer 5 at $3 \times 10^{14} cm^{-2}$, 30keV. Thereby, surfaces of the single silicon layer 5 become amorphous.

Next, a titanium layer 21 which has a thickness of 15nm as a metallic layer is formed on the SOI substrate by a sputtering method, as shown in Fig.7. A cobalt layer or a nickel layer can be used for the metallic layer instead of the titanium layer.

A thickness of the titanium layer 21 is set to an appropriate thickness according to a depth of the active region, that is, a depth of the single silicon layer 5. In this embodiment, as a depth of the active region in the fully depletion type SOI is less than 50nm, a thickness of a metallic silicide layer, such as titanium silicide which is formed in the active region is necessary to be less than the depth of the active region, that is, the single silicon layer. A thickness of the metallic silicide layer becomes 2.5 times of the thickness of the metallic layer, such as the titanium layer. In this embodiment, a thickness of titanium layer 21 is set to 15nm.

Collimate sputtering method or Long Throw sputtering method is used for forming the titanium layer 21. In these methods, metal from a metallic target can be straightly sputtered to the SOI substrate.

In the Collimate sputtering method, a collimate plate PC is arranged between a metallic target T and a semiconductor wafer SUB, as shown in Fig.11(b). Thereby, metallic particles among all sputtered metallic particles, which have small angle of incidence can be reached to the semiconductor wafer SUB.

In the Long Throw method shown in Fig.11(c), an interval between a metallic target and a semiconductor wafer SUB is longer that that of a general sputtering method shown in Fig.11(a). In the general sputtering method, the interval is set to 60nm. On the other hand, the interval of the Long Throw method is set to 340nm. Further, a vacuum level of the Long Throw method is higher than that of the general sputtering method for enhancing straight-forwardness of the sputtered metallic particles. Metallic particles which have large angle of incidence larger than θ can not reach to the semiconductor wafer SUB in this Long Throw method. As an average of free path of the sputtered metallic particles can be longer by the high vacuum level, a scatter of the metallic particle can be reduced.

The SOI substrate is kept at a temperature of 300℃ during forming of the titanium layer 21 by the Collimate or the Long Throw method.

Here, a x-ray diffraction of the titanium layer formed on the substrate which is kept at temperatures of 200℃, 300℃, 400℃ and a room temperature (25℃) using the Long Throw sputtering method, is shown in Fig.12. Referring to Fig.12, under a temperature of 300℃, the higher a temperature of the substrate is, the stronger an orientation of (200) surface of the titanium layer becomes. An orientation of (200) surface is weak at a temperature of 400℃. Therefore, a crystalline structure of a titanium layer which is formed at a temperature between 200℃ and 400℃, differs from a crystalline structure which is formed at under 200℃ or over 400℃.

Returning to Fig.7, a titanium nitride layer 23 having a thickness of 30nm is formed on the titanium layer 21, which is continuous with forming the titanium layer 21 without exposing the SOI substrate to the air. The titanium layer 21 and the titanium nitride layer 23 are preferred to form successively in the same process chamber.

As the titanium nitride 23 is successively formed on the titanium layer 21 as a protective layer, the titanium layer 21 is protected from an oxidation. That is, the titanium layer which is easy to be oxidized, can be protected against a fall of quality of the titanium layer due to the oxidation. As a result, the titanium nitride layer 23 has a function of isolating the titanium layer 21 from an external oxide atmosphere. A tungsten layer can be used for the protective layer instead of the titanium nitride layer.

In this embodiment, a thickness of the protective layer, such as the titanium nitride layer 23 is thicker than that of the metallic layer, such as the titanium layer 21, for protecting the metallic layer from the oxidation. Further, the protective layer is preferred to have a thickness more than 30nm for restraining from incursion of external oxygen.

Then, a first heat treatment is carried out. That is, the SOI substrate on which the titanium layer 21 and the titanium nitride layer 23 are formed, is heated to a temperature of 750℃ in an atmosphere of nitrogen. Thereby, titanium silicide layers 31, 32, 33 which have a thickness of 30nm respectively

are formed in interface surfaces, as shown in Fig.8. The titanium silicide layers 31, 32, 33 are respectively formed on the interface surfaces between the titanium layer 21 and the active regions and the gate electrode 11. Such titanium silicide layers 31, 32, 33 are composed of a Ti-Si layer which has a composition ratio of titanium and silicon that is 1:1 or a Ti_2Si layer which includes more titanium than silicon. So, resistance of the titanium silicide layers 31, 32, 33 is high. That is, the titanium layers 31, 32, 33 have a crystalline structure of C49.

Then, the titanium nitride layer 23 and the titanium layer 32 which is not reacted with silicon in the single silicon layer 5 or the gate electrode 11, is removed using mixture liquid of an ammonia solution and a hydrogen peroxide solution, as shown in Fig. 9.

Then, a second heat treatment is carried out. That is, the titanium silicide layers 31, 32, 33 are heated to a temperature of 850℃. Thereby, the TiSi layer or the Ti_2Si layer of the titanium silicide layers 31, 32, 33 are respectively changed into $TiSi_2$ layers 41, 42, 43, as shown in Fig.10. That is, the titaniumu layers ($TiSi_2$) 41, 42, 43 have a crystalline structure of C54. Therefore, as resistance of

the titanium silicide layers 41, 42, 43 become low, resistance of the gate electrode 11 and the active regions can be reduced. As thickness of the titanium silicide layers 42, 43 which are formed in the active region (the source and drain regions) is 30nm, portions of the titanium silicide layers 42, 43 do not reach to the silicon oxide layer 3.

Then, an intermediate layer, contact holes and conductive lines are formed on the base for forming MOS transistors.

Although the titanium silicide layers of the preferred embodiment are very thin (30nm), the titanium silicide layers 41, 42, 43 have low regular sheet resistance of about 10Ω/sq, as shown in Fig.13. Further, the sheet resistance of this embodiment is independent of width of titanium silicide layer.

In Fig.13, black circles denote a relation between width of silicide layer and sheet resistance of the preferred embodiment. Further, white triangles denote a similar relation of the conventional silicide layer which has a thickness of 30nm.

According to the present invention, a SALICIDE method for forming

metallic silicide layers can be applied to a semiconductor substrate which has a thin silicon layer such as a SOI substrate. Particularly, in a fully depleted SOI structure which has a very thin single silicon layer, metallic silicide layers can be formed precisely.

As a result, according to the present invention, a semiconductor device having a thin metallic silicide layer can be formed with reducing a sheet resistance by thin wire effect.

In the above embodiment, argon ions can be implanted into the SOI substrate instead of the arsenic ions, as shown in Fig.14. Such argon ions Ar + are implanted into the single silicon layer 5 at $5x10^{14}cm^{-2}$, 15keV. Thereby, surfaces of the single silicon layer 5 become amorphous. As the implanted argon ions in the substrate are not neither a p type impurity nor n type impurity, the argon ions have no serious effect in the active region in which p channel or n channel type transistors are formed. As a result, the transistors can be precisely formed in the active region.

The present invention has been described above with reference to

illustrative embodiments. However, this description must not be considered to be confined only to the embodiments illustrated. Various modifications and changes of these illustrative embodiments and the other embodiments of the present invention will become apparent to one skilled in the art from reference to the description of the present invention. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.